CONF\_REG\_CRC\_DET IP SPEC

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## Introduction

Check the CRC value of configure registers and MTP shadow registers every 2ms, if no right, output CONF\_REG\_CRC\_FLT is high.

## Feature

Monitor the configure registers and MTP shadow register to ensure all values are right.

## Register Definition

### Register Map

Table 1 CONF\_REG\_CRC\_DET Register Map

|  |  |  |  |  |  |  |  |  |  |  |
| --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- |
| **Name** | **Add** | **D7** | **D6** | **D5** | **D4** | **D3** | **D2** | **D1** | **D0** | **default** |
| CONF\_ CRC\_H | 0x2000 | CONF\_CRC[15:8] | | | | | | | | 0x00 |
| CONF\_ CRC\_L | 0x2001 | CONF\_CRC[7:0] | | | | | | | | 0x00 |
| SYS\_FLT2 | 0x5114 |  |  | CONF\_CRC |  |  |  |  |  | 0x00 |

## Functional Details

### Block Diagram

The following diagram shows the CONF\_REG\_CRC\_DET inputs and outputs.



Figure1 CONF\_REG\_CRC\_DET diagram

### Module input/output list

|  |  |  |  |  |
| --- | --- | --- | --- | --- |
| Name | Dir | Width | Discirption | duration |
| CONF\_REG\_CRC\_FLT | O | 1 | Configuration register crc fault bit | Level(CLK\_SLOW2 domain) |
| CLK\_SLOW2\_SC | I | 1 | Redundant CLK\_SLOW | 256KHz, 50%duty |
| resetb\_SR\_CLK\_SLOW | I | 1 | Scan\_muxed resetb and soft resetb for CLK\_SLOW domain | level |
| load\_done | I | 1 | MTP load done | Level(CLK\_MTP domain) |
| pulse\_SLOW2\_2ms | I | 1 | 2ms pulse in CLK\_SLOW2 domain | 1 CLK\_SLOW2 |
| reg0000~001E | I | 8\*31 | Configuration registers 0000~001E | Level(CLK\_REG domain) |
| reg0100~0117 | I | 8\*24 | Configuration registers 0100~0117 | Level(CLK\_REG domain) |
| TM\_REG1~TM\_REG10 | I | 8\*10 | Configuration registers 0800~0809 | Level(CLK\_REG domain) |
| reg1000~107F | I | 8\*128 | Configuration registers 1000~107F  (MTP shadow registers) | Level(CLK\_REG domain) |
| CONF\_CRC | I | 16 | Configuration registers 2000~2001 | Level(CLK\_REG domain) |

### Clock Domain

The clock for CONF\_REG\_CRC\_DET is CLK\_SLOW2\_SC. (HWSR2\_CONF\_REG\_CRC\_DET)

### CONF\_REG\_CRC\_DET function description

IBM algorithm with polynomial (x16+x15+x2+1) and default value 16’hFFFF is used for CRC. CONFIG\_adr[13:0] is defined that goes through all configuration registers and MTP shadow registers, i.e., 16’h0000~16’h001E, 16’h0100~0117, 16’h0800~0809, 16’h1000~107F and 16’h 2000~2001.

CONFIG\_data[7:0] changes to corresponding register value every time CONFIG\_adr changes.

CRC calculator updates every time CONFIG\_data[7:0] changes. Once CONFIG\_adr[13:0] went through all the registers, check the calculator result, if not 0, CONF\_REG\_CRC\_FLT is high.

(HWSR1\_CONF\_REG\_CRC\_DET)